ABSTRACT

A short-channel NMOS transistor in a p-well, bordered laterally on each side by an isolation region and vertically by a channel stop region, has a n-source and a n-drain, each comprising a shallow region extending to the transistor gate and a deeper region recessed from the gate, and both having a depletion region when reverse biased. The shallow regions are surrounded in part by an enhanced p-doping implant pocket. The transistor further has in these regions of enhanced p-doping another region of a p-resistivity higher than the remainder of the semiconductor. These regions extend laterally approximately from the inner border of the respective shallow region to the inner border of the respective recessed region, and vertically from a depth just below the depletion regions of source and drain to approximately the top of the channel stop regions.

According to the invention, these regions of higher p-type resistivity are created after gate definition by an ion implant of compensating n-doping, such as arsenic or phosphorus, using the same photomask already used for implants creating the extended source and drain and the pockets of enhanced p-doping.

In an ESD event, these regions of higher resistivity increase the current gain of the parasitic lateral npn bipolar transistor and thus raise the current It2, which initiates the thermal breakdown with its destructive localized heating, thereby improving ESD robustness.